Efficient front-end power

Bringing efficiency, cost, and volume together is a major balancing act, and getting the right percentage is essential

By MIKE WAGNER and MOSHE DOMB
Cherokee International
Tustin, CA
http://www.cherokeepwr.com

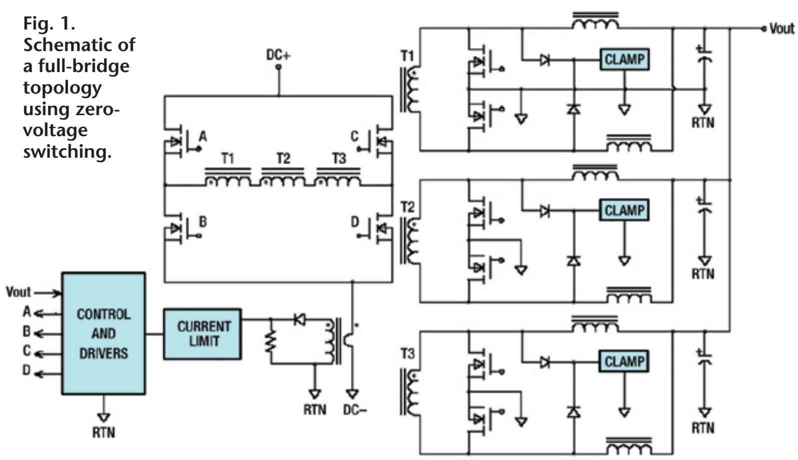
As end applications demand more and more processing power, increased bandwidth, and more storage capacity, datacenters are under fire to manage and support these needs while balancing energy conservation and operating costs. These demands draw more power, making it harder to thermally cool the end equipment as computing power continues to rise. One key electrical component with respect to these issues, which is also at the heart of every server, is located in the power train — namely the front end or ac to 12-Vdc power supply that powers other devices downstream.

To see the impact of these issues, you have to dissect the power-train into its components and get a true understanding of how they are used in practice. The typical server tends not to operate at full or near 100% load capacity but rather at 20% to 30% of the front end's full-load operating performance.

This is primarily due to two points. First, the way the ac/dc front ends are configured in either an n+1 or n+n redundant architecture, and second, the true draw of load that the server requires to carry out it's functions. Often a server is not heavily taxed. Its power draw is only a small percentage of the full rating of the ac front end even though it is sized or specified for 100% of its capacity.

The drawback to this point is that the ac/dc front end suffers dramatically in terms of its efficiency performance, a magnitude of more than a 10% to 15% drop versus its full load rating. This becomes an issue in a datacenter where the excess in dissipation is multiplied by the number of servers installed, making it economically undesirable to operate them in this manner. For the highest level of redundancy and reliability — a Tier 4 data center — for every kilowatt used for processing, some $22,000 is spent on power and cooling infrastructure.

Fig. 1. Schematic of a full-bridge topology using zero-voltage switching.



The power supply industry has historically maximized power density per-design, peaking the efficiency at approximately 70% to 80% of load in order to provide full power in a given volume — allowing the 20% to 50% light-load area to suffer at its expense.

Topology selection and baseline efficiency improvement

Most ac/dc high-performance front ends already use zero-voltage-switching (ZVS) full-bridge switching techniques. However, applying these circuits innovatively can provide flexibility, improved thermal management, and a reliable design approach as well as efficient performance.

One approach uses the full bridge with ZVS in a "current-doubler" configuration with three secondary stages. In *Fig. 1*, the primary side shows three transformers connected in a series.

On the secondary-side topology, these parallel and identical sections are designed in parallel versus a single transformer. The benefit of this patent-pending approach is an even transfer of energy from the primary to the secondary of each stage given that each of three primary windings are in a series. This results in equal dissipation and equal thermal balancing as well as inherent current sharing between each secondary stage.

The secondary also uses a proprietary clamp design that acts to recover the energy associated with reverse current of the output synchronous rectifiers normally dissipated as heat. This design allows for approximately 90% of this energy to be recovered and reused in the circuit as recycled energy.

Where to gain overall efficiency points

Redesigning the main topology addresses efficiency, power density and heat management. Those are all key points, yet there are other overall efficiency gains to be had elsewhere in the power supply via various technical approaches. The right PFC circuit with a ZVS can get an additional 1% efficiency gain.

A second area, a full-bridge design that switches into three parallel secondaries coupled with high (400-kHz) frequency, can result in a very-low-output choke, very low core and copper losses, and very small footprint size and still maintain losses to provide an additional 1% efficiency gain. The secondary circuit using a current doubler concept can eliminate thermal stress to balance heat and gain an additional 2% efficiency.

And finally, the optimization of hold up time can gain the design another 1%. Adding all these areas together, you can achieve a very flat efficiency curve.

Fine-tuning the PFC stage

Power supply efficiency is already ultra high in comparison to the levels just a few years back. To find the last few incremental percentage gains to get closer to 100% efficiency, designers are now forced to break sections up and look at the minutia. In the PFC stage, using zero voltage switching is an element to be considered in the design.

Additionally, a proprietary circuit is used to eliminate the reverse recovery of the PFC main diode along with achieving nearly zero turn-off loss for the MOSFETs.

Light-load efficiency

In reality, many data centers run their equipment at light load though power supplies (in the past) have been, by request, designed for efficiency at full load. Achieving a high efficiency of 90% or more at light load is a daunting challenge that needs to be carefully addressed.

There is not one magic solution to implement, but rather a combination of individual steps that can boost the efficiency performance at light load while not sacrificing full-load performance. The first step is to create a baseline, a model of each stage of the design, so that the designer can tackle areas that lead to the biggest gains at light load levels.

Here are some steps to improve light-load performance (see *Fig. 2*):

1. The immediate area for the biggest gain would be to optimize the switching frequency for the full bridge and the PFC circuit. This point is similar to the discussion earlier in this article. However, for light-load efficiency, a lower frequency of operation, measured in kilohertz, for the PFC stage actually does the job and allows for a half-percent efficiency gain without sacrificing PFC performance or distortion of harmonic-current content.

2. Housekeeping circuitry becomes a very high percentage of overall losses when looking at light-load efficiency as opposed to being a low percentage at full load. Here, managing the minutia is key. For housekeeping, the internal bias supply and the fan power supply can be controlled to use less voltage and dissipate less power. Normally for a high-power 1U power supply, two fans are employed with each fan dissipating 15 W. At light load, this can be reduced by 50% to 7 W.

Using the intelligence of the microcontroller for adjusting fan-speed control thus brings another half-percent efficiency gain.

3. Reducing the preload losses at the point of no load brings another few tenths of a percent.

4. The magnetic design of the main transformers and the output choke can both be designed to reduce the core losses — static, not switching — which at the light-load level account for a larger proportion of the inefficiency.

5. Dead-time optimization as a function of load is another important area for finding efficiency gains. In a full bridge with ZVS, the ZVS loss (Pzvs) can be major: $P_{ZVS} = 1/2(C_{OSS} * Vds^2 * freq)$.

By allowing more dead time, the drain source resonates down to zero before it is turned on again. Then, the switching losses (P_{zvs}) can be substantially reduced at light load. On the other hand, at full load, the efficiency is higher at the shortest dead time.

There is also a need to control the dead time over different operating points. This is another application where digital supervision, through the use of a micro-controller, can achieve both sets of goals by optimizing the dead-time versus load and enhance efficiency performance.

6. Shutting down synchronous MOSFETs not required at light load reduces the bias power needed to drive the MOSFET gates. The power related to the drive is calculated by $P_{drive} = n*V_{CC}*Q_{gstotal}*freq$. For example, Cherokee's CAR2512 has n = 24 synchronous MOSFETs, and reducing them to n = 12 at 50% of the load saves about 8 W (see *Fig. 2*).

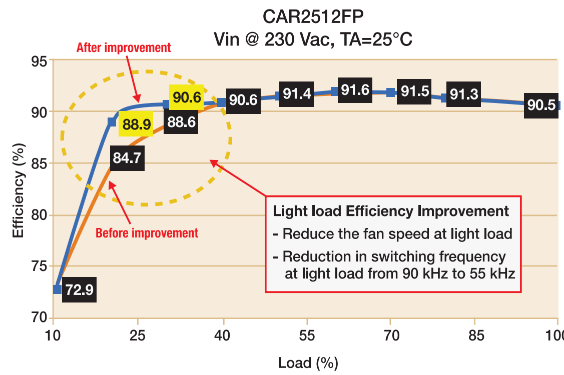


Fig. 2. Efficiency before and after implementing steps of light-load efficiency improvement.

7. The ZVS range is extended by adding an inductor L_{res}, which stores the primary current and extends the range of ZVS based on the following equation: $1/2(L_{res} + L_{leakage}) * Ipri^2 = 1/2(2*C_{OSS}*380V^2)$ where L_{eakage} is the combined leakage inductance of all transformers in series A, and $2*C_{OSS}$ is the equivalent capacitance of the top and bottom primary FETs.

Efficiency, cost, volume

Bringing efficiency, cost, and volume together is a major balancing act. However, getting the right percentage increase in efficiency in the right form factor with the right quality output, performance and cost is what the design engineer must appropriately choose.